IN THE CLAIMS

1. (Currently Amended) A delay time adjusting method of adjusting a delay time of an input signal so that a phase of said input signal and a phase of an output signal match each other, the method comprising the steps of:

comparing phases of said output signal and said input signal with each other; and

starting an increase of the delay time ~~at any time when~~ whenever a phase difference is detected in the step of comparing.

2. (Original) The delay time adjusting method as claimed in claim 1, further comprising a step of producing said output signal by delaying said input signal by a DLL circuit.

3. (Previously Presented) A delay time adjusting method comprising:

comparing the phases of an input first periodic signal and an output second periodic signal;

adjusting a delay time of the input first periodic signal so that a phase of the input first periodic signal and a phase of the output second periodic signal match within a predetermined tolerance, wherein

when a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a predetermined rising edge of said input first periodic signal, said delay time is adjusted so that said predetermined rising edge of said output second periodic signal matches a rising edge of said input first periodic signal, a phase

of the rising edge being behind and nearest to said phase of said predetermined rising edge of said output second periodic signal, and wherein the adjusting of said delay at an initial stage of the adjusting is to increase said delay when starting the step of adjusting of said delay.

4. (Previously Presented) A delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the method comprising:

a first step of judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of said input first periodic signal; and

a second step of increasing the delay time to adjust said phase of said output second periodic signal so that, when said phase of said predetermined rising edge is judged to be behind said phase of said first rising edge in said first step, said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal match each other, the second rising edge being one period behind said first rising edge, wherein the step of delaying at an initial stage of adjustment is to increase the delay time when starting the delay time adjustment.

5. (Currently Amended) A delay time adjusting circuit for adjusting a delay time of an input signal so that a phase of said input signal and a phase of an output

signal match each other between phases based on a comparison of said input signal and said output signal, the circuit comprising:

a detecting ~~means~~ circuit for detecting a phase difference between said phase of said input signal and said phase of said output signal; and

a delaying ~~means~~ circuit for increasing a delay time of said phase of said output signal, when starting the delay time adjustment, ~~until~~ so that the delay time is set to a value at which said phase difference becomes N periods, where N is an integer other than zero.

6. (Currently Amended) A delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the circuit comprising:

a judging ~~means~~ circuit for judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a predetermined rising edge of said input first periodic signal; and

a delaying ~~means~~ circuit for adjusting said delay time so that, when said phase of said predetermined rising edge of said output second periodic signal is judged to be behind said phase of said predetermined rising edge of said input first periodic signal by said judging ~~means~~ circuit, said predetermined rising edge of said output second periodic signal matches a rising edge of said input first periodic signal, a phase of the rising edge being behind and nearest to said phase of said predetermined rising edge of

said output second periodic signal, wherein the step of delaying at an initial stage of adjustment is to increase the delay time when starting the delay time adjustment.

7. (Currently Amended) A delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the circuit comprising:

a delaying ~~means~~ circuit for delaying said input first periodic signal so as to generate said output second periodic signal;

a phase-detecting ~~means~~ circuit for detecting whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of said input first periodic signal; and

an adjusting ~~means~~ circuit for controlling said delaying ~~means~~ circuit so that, when said phase of said predetermined rising edge is judged to be behind said phase of said first rising edge by said phase-detecting ~~means~~ circuit, said delaying ~~means~~ circuit delays said phase of said output second periodic signal until said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal match each other, the second rising edge being one period behind said first rising edge, wherein the step of delaying at an initial stage of adjustment is to increase the delay time when starting the delay time adjustment.

8. (Currently Amended) The delay time adjusting circuit as claimed in claim 7, wherein said adjusting ~~means~~ circuit controls said delaying ~~means~~ circuit so that, after said phase of said predetermined rising edge and said phase of said second rising edge match each other, said phase of said predetermined rising edge and said phase of said second rising edge match each other all the time within a tolerable range.